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09/648,153	08/25/2000	Jun Koyama	740756-2204	6963

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EXAMINER	
MOON, SEOKYUN	

ART UNIT	PAPER NUMBER
2629	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	09/648,153	KOYAMA, JUN	
	Examiner	Art Unit	
	SEOKYUN MOON	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 February 2012*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

4)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

5)☒ Claim(s) *6,8-14,17-22,24-27,29 and 47-50* is/are pending in the application.

5a) Of the above claim(s) _____ is/are withdrawn from consideration.

6)☐ Claim(s) _____ is/are allowed.

7)☒ Claim(s) *6,8-14,17-22,24-27,29,47-50* is/are rejected.

8)☐ Claim(s) _____ is/are objected to.

9)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

10)☐ The specification is objected to by the Examiner.

11)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

12)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date *2/8/2012*.
4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Remarks

As a preliminary matter, Examiner respectfully submits that the examiner assigned to examine the instant Application has been changed.

Response to Arguments

Applicant's arguments filed February 8, 2012 have been fully considered.

Regarding the newly amended claim 6, Applicant argues (*See* Remarks, p. 8),

> "Applicant continues to contends that Parks, Hoshi, Runaldue and/or Johary, taken alone or in combination, fail to disclose, suggest or render obvious independent claims 6, 12, 18, 24, particularly in light of the above features.".

Examiner respectfully disagrees.

Examiner respectfully submits that Parks, Runaldue, and Hoshi, in combination, teach the limitation of claim 6. A detailed explanation as to how the combination of the cited prior arts teaches the claim limitation is provided below.

Claim Rejections - 35 USC § 103

The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

Claims 6, **8**, **11**, **18**, **19**, **22**, **47**, and **49** are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 5,471,225 by Parks in view of U.S. Patent No. 5,325,338 by Runaldue et al. (herein after, "Runaldue") and Japanese Patent No. 58-143389 by Hoshi.

As to **claim 6**, Parks teaches an active matrix display device [abs. the last two lines and fig. 5] comprising an electro-optical modulating layer [abs., ll. 1-4, the liquid crystal layer of the "LCD"] disposed between a pair of substrates [fig. 2, "22" and "24"], said active matrix display device comprising:

a plurality of column lines [fig. 5, "32"] and a plurality of row lines [fig. 5, "34"] supported by one of the substrates and defining a plurality of pixels [fig. 2] in a matrix form;

a plurality of pixel electrodes [fig. 5, "36"] formed in said plurality of pixels and supported by said one of said substrates [fig. 2];

a thin film transistor [fig. 5, "38"] disposed in each of said pixels and electrically connected to one of said column lines [fig. 5, "32"] and one of said row lines [fig. 5, "34"];

a memory circuit [fig. 5, "50" excluding "38"] disposed in each of said pixels and electrically connected to said thin film transistor [fig. 5, "38"], wherein said memory circuit stores an information output by said thin film transistor [col. 6, ll. 5-18], wherein the memory circuit comprises a pair of inverters [fig. 5, the combination of "R1" and "52", and the combination of "R2" and "54", and col. 6, ll. 53-56], each of the inverters comprising **a transistor** and **a resistor**, wherein an input of one of the pair of inverters [fig. 5, the combination of "R1" and "52"] is connected to the thin film transistor [fig. 5, "38"] and an output of the other one of the pair of inverters [fig. 5, the combination of "R2" and "54"], and wherein an output of the one of the pair of inverters [fig. 5, the combination of "R1" and "52"] is connected to an input of the other one of the pair of inverters [fig. 5, the combination of "R2" and "54"] and one of the plurality of pixel electrodes [fig. 5, "36"];

at least two voltage source lines (*See* Fig. 5 and *note* that it is required to have a line/electrode for each of power and ground voltage sources to provide power to each of a plurality of pixels) electrically connected to said memory circuit [fig. 5, "50" excluding "38"] wherein the pair of inverters [fig. 5, the combination of "R1" and "52", and the combination of "R2" and "54", and col. 6, ll. 53-56] are connected between the two voltage source lines: and

an opposite electrode [fig. 2, "common electrode 30"] on the other of said substrates [fig. 2, "22"],

wherein different voltages [fig. 5, power and ground connected to "R1" and "R2", and "52" and "54"] supplied to the two voltage source lines are applied to said pixel electrode through the pair of inverters based on the information stored by the corresponding memory circuit.

Parks does not teach that each of the inverters comprises an n-channel thin film transistor and a p-channel thin film transistor.

However, Runaldue teaches the concept of forming each of a pair of inverters [fig. 3, "inverter 94" and "inverter 98"] by using an n-channel thin film transistor [fig. 3, "101" or "103"] and a p-channel thin film transistor [fig. 3, "100" or "102"].

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify each of the inverters of Parks to include an n-channel thin film transistor and a p-channel thin film transistor instead of a transistor and a resistor and to have the configuration of Runaldue's pair of inverters, as taught by Runaldue, in order to achieve the predictable result of providing a signal storing function in the pixels of Parks with reduced power consumption.

Parks as modified by Runaldue does not teach that an AC voltage having an amplitude equivalent to that of the voltages output of the memory circuit is supplied to the opposite electrode.

However, Hoshi teaches the concept of providing an AC voltage [fig. 3a, "12b"] having an amplitude equivalent to that of the voltage output [fig. 3a, "12a"] of a memory circuit [fig. 2, "7" and "8"] in an active matrix display device [fig. 2] to an opposite electrode [fig. 2, the electrode corresponding to the bottom portion of "9"] of the display device [col. 5, the last eight lines].

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to output a first AC voltage from the memory circuit of Parks as modified by Runaldue and to output a second AC voltage having an amplitude equivalent to that of the voltage output of the first AC voltage from the opposite electrode, as taught by Hoshi, in order to achieve the predictable result of reducing power consumption and preventing the degradation of the electro-optical modulating layer.

As to **claim 8**, Parks teaches that the number of pixel electrodes [fig. 5, "36"] equals the number of the digital memory circuits [fig. 5, "50" excluding "38"].

As to **claim 11**, Parks teaches that the different voltages [fig. 5, power and ground connected to "R1" and "R2", and "52" and "54"] include a high voltage and a low voltage.

As to **claim 18**, Parks teaches an active matrix display device [abs. the last two lines and fig. 5] comprising an electro-optical modulating layer [abs., ll. 1-4, the liquid crystal layer of the "LCD"] disposed between a pair of substrates [fig. 2, "22" and "24"], said active matrix display device comprising:

a plurality of column lines [fig. 5, "32"] and a plurality of row lines [fig. 5, "34"] supported by one of the substrates and defining a plurality of pixels [fig. 2] in a matrix form;

a plurality of pixel electrodes [fig. 5, "36"] formed in said plurality of pixels and supported by said one of said substrates [fig. 2];

a first thin film transistor [fig. 5, "38"] disposed in each of said pixels and electrically connected to one of said column lines [fig. 5, "32"] and one of said row lines [fig. 5, "34"];

a memory circuit [fig. 5, "50" excluding "38"] disposed in each of said pixels and electrically connected to said first thin film transistor [fig. 5, "38"], wherein said memory circuit stores an information output by said first thin film transistor [col. 6, ll. 5-18],

at least two voltage source lines (*See* Fig. 5 and *note* that it is required to have a line/electrode for each of power and ground voltage sources to provide power to each of a plurality of pixels) electrically connected to said memory circuit [fig. 5, "50" excluding "38"]; and

an opposite electrode [fig. 2, "common electrode 30"] on the other of said substrates [fig. 2, "22"],

wherein different voltages [fig. 5, power and ground connected to "R1" and "R2", and "52" and "54"] supplied to the two voltage source lines are applied to said pixel electrode based on the information stored by the corresponding memory circuit,

wherein said memory circuit comprises at least two inverters [fig. 5, the combination of "R1" and "52", and the combination of "R2" and "54", and col. 6, ll. 53-56], said inverters comprising at least one transistor and one resistor and being connected with said voltage source lines; and

wherein an input of one of the pair of inverters [fig. 5, the combination of "R1" and "52"] is connected to the first thin film transistor [fig. 5, "38"] and an output of the other one of the pair of inverters [fig. 5, the combination of "R2" and "54"], and wherein an output of the one of the pair of inverters is connected to an input of the other one of the pair of inverters and one of the plurality of pixel electrodes [fig. 5, "36"], and

wherein two inverters [fig. 5, the combination of "R1" and "52", and the combination of "R2" and "54", and col. 6, ll. 53-56] are connected between the two voltage source lines.

Parks does not teach that each of the inverters comprises at least two thin film transistors.

However, Runaldue teaches the concept of forming each of a pair of inverters [fig. 3, "inverter 94" and "inverter 98"] by using two thin film transistors [fig. 3, "101" or "103", and "100" or "102"].

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify each of the inverters of Parks to include two thin film transistors instead of a transistor and a resistor and to have the configuration of Runaldue's pair of inverters, as taught by Runaldue, in order to achieve the predictable result of providing a signal storing function in the pixels of Parks with reduced power consumption.

Parks as modified by Runaldue does not teach that an AC voltage having an amplitude equivalent to that of the voltages output of the memory circuit is supplied to the opposite electrode.

However, Hoshi teaches the concept of providing an AC voltage [fig. 3a, "12b"] having an amplitude equivalent to that of the voltage output [fig. 3a, "12a"] of a memory circuit [fig. 2, "7" and "8"] in an active matrix display device [fig. 2] to an opposite electrode [fig. 2, the

electrode corresponding to the bottom portion of "9"] of the display device [col. 5, the last eight lines].

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to output a first AC voltage from the memory circuit of Parks as modified by Runaldue and to output a second AC voltage having an amplitude equivalent to that of the voltage output of the first AC voltage from the opposite electrode, as taught by Hoshi, in order to achieve the predictable result of reducing power consumption and preventing the degradation of the electro-optical modulating layer.

As to **claim 19**, Parks teaches that the number of pixel electrodes [fig. 5, "36"] equals the number of the memory circuits [fig. 5, "50" excluding "38"].

As to **claim 22**, Parks teaches that the different voltages [fig. 5, power and ground connected to "R1" and "R2", and "52" and "54"] include a high voltage and a low voltage.

As to **claim 47**, Parks teaches that said electro-optical modulating layer comprises a liquid crystal [abs., l. 1].

As to **claim 49**, Parks teaches that said electro-optical modulating layer comprises a liquid crystal [abs., l. 1].

Claims 9, **10**, **20**, and **21** are rejected under 35 U.S.C. 103(a) as being unpatentable over Parks, Runaldue, and Hoshi as applied to claims 6, 8, 11, 18, 19, 22, 47, and 49 above, and further in view of U.S. Patent No. 5,196,839 by Johary et al. (herein after, "Johary").

As to **claims 9** and **10**, Parks as modified by Runaldue and Hoshi does not expressly teach that the active matrix display device includes a digital and time gradation display device.

However, Johary teaches the concept of generating a digital [fig. 1d] and time gradation signal [fig. 1c] as the display signal for a display device.

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify the active matrix display device of Parks as modified above to use a digital and time gradation signal as the display signal, as taught by Johary, in order to provide an effective visual differentiation for displayed images [Johary, col. 1, ll. 28-32].

As to **claims 20** and **21**, Parks as modified by Runaldue and Hoshi does not expressly teach that the active matrix display device includes a digital and time gradation display device.

However, Johary teaches the concept of generating a digital [fig. 1d] and time gradation signal [fig. 1c] as the display signal for a display device.

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify the active matrix display device of Parks as modified above to use a digital and time gradation signal as the display signal, as taught by Johary, in order to provide an effective visual differentiation for displayed images [Johary, col. 1, ll. 28-32].

Claims 12-14, **17**, **24-26**, **29**, **48**, and **50** are rejected under 35 U.S.C. 103(a) as being unpatentable over Parks in view of Hoshi.

As to **claim 12**, Parks teaches an active matrix display device [abs. the last two lines and fig. 5] comprising an electro-optical modulating layer [abs., ll. 1-4, the liquid crystal layer of the "LCD"] disposed between a pair of substrates [fig. 2, "22" and "24"], said active matrix display device comprising:

a plurality of column lines [fig. 5, "32"] and a plurality of row lines [fig. 5, "34"] supported by one of the substrates and defining a plurality of pixels [fig. 2] in a matrix form;

a plurality of pixel electrodes [fig. 5, "36"] formed in said plurality of pixels and supported by said one of said substrates [fig. 2];

a first thin film transistor [fig. 5, "38"] disposed in each of said pixels and electrically connected to one of said column lines [fig. 5, "32"] and one of said row lines [fig. 5, "34"];

a memory circuit [fig. 5, "50" excluding "38"] disposed in each of said pixels and electrically connected to said thin film transistor [fig. 5, "38"], wherein said memory circuit stores an information output by said thin film transistor [col. 6, ll. 5-18],

at least two voltage source lines (*See* Fig. 5 and *note* that it is required to have a line/electrode for each of power and ground voltage sources to provide power to each of a plurality of pixels) electrically connected to said memory circuit [fig. 5, "50" excluding "38"]; and

an opposite electrode [fig. 2, "common electrode 30"] on the other of said substrates [fig. 2, "22"],

wherein different voltages [fig. 5, power and ground connected to "R1" and "R2", and "52" and "54"] supplied to the two voltage source lines are applied to said pixel electrode based on the information stored by the corresponding memory circuit, and

wherein said memory circuit comprises at least second [fig. 5, "54"] and third thin film transistors [fig. 5, "52"],

one of source or drain of the second thin film transistor [fig. 5, "54"] being connected with one of said voltage source lines [fig. 5, the line delivering the power to the resistor "R2"], a

gate electrode of the third thin film transistor [fig. 5, "52"], and one of source or drain of the first thin film transistor [fig. 5, "38"],

the other of source or drain of the second transistor [fig. 5, "54"] being connected with the other of said voltage source lines [fig. 5, the line delivering the ground to "54"] and one of source or drain of the third thin film transistor [fig. 5, "52", note that all grounds are connected] and

a gate electrode of the second thin film transistor [fig. 5, "54"] being connected with the other of source or drain of the third thin film transistor [fig. 5, "52"], one of said voltage source lines, and said pixel electrode [fig. 5, "36"].

Parks does not teach that an AC voltage having an amplitude equivalent to that of the voltages output of the memory circuit is supplied to the opposite electrode.

However, Hoshi teaches the concept of providing an AC voltage [fig. 3a, "12b"] having an amplitude equivalent to that of the voltage output [fig. 3a, "12a"] of a memory circuit [fig. 2, "7" and "8"] in an active matrix display device [fig. 2] to an opposite electrode [fig. 2, the electrode corresponding to the bottom portion of "9"] of the display device [col. 5, the last eight lines].

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to output a first AC voltage from the memory circuit of Parks and to output a second AC voltage having an amplitude equivalent to that of the voltage output of the first AC voltage from the opposite electrode, as taught by Hoshi, in order to achieve the predictable result of reducing power consumption and preventing the degradation of the electro-optical modulating layer.

As to **claim 13**, Parks as modified by Hoshi teaches that a voltage supplied to the electro-optical modulating layer is substantially zero on time average [Hoshi, figs. 3a-3b].

As to **claim 14**, Parks as modified by Hoshi teaches that the number of pixel electrodes [Parks, fig. 5, "36"] equals the number of the memory circuits [Parks, fig. 5, "50" excluding "38"].

As to **claim 17**, Parks teaches that the different voltages [Parks, fig. 5, power and ground connected to "R1" and "R2", and "52" and "54"] include a high voltage and a low voltage.

As to **claim 24**, Parks teaches an active matrix display device [abs. the last two lines and fig. 5] comprising an electro-optical modulating layer [abs., ll. 1-4, the liquid crystal layer of the "LCD"] disposed between a pair of substrates [fig. 2, "22" and "24"], said active matrix display device comprising:

a plurality of column lines [fig. 5, "32"] and a plurality of row lines [fig. 5, "34"] supported by one of the substrates and defining a plurality of pixels [fig. 2] in a matrix form;

a plurality of pixel electrodes [fig. 5, "36"] formed in said plurality of pixels and supported by said one of said substrates [fig. 2];

a first thin film transistor [fig. 5, "38"] disposed in each of said pixels and electrically connected to one of said column lines [fig. 5, "32"] and one of said row lines [fig. 5, "34"];

a memory circuit [fig. 5, "50" excluding "38"] disposed in each of said pixels and electrically connected to said thin film transistor [fig. 5, "38"], wherein said memory circuit stores an information output by said first thin film transistor [col. 6, ll. 5-18],

at least two voltage source lines (*See* Fig. 5 and *note* that it is required to have a line/electrode for each of power and ground voltage sources to provide power to each of a

plurality of pixels) electrically connected to said memory circuit [fig. 5, "50" excluding "38"]; and

an opposite electrode [fig. 2, "common electrode 30"] on the other of said substrates [fig. 2, "22"],

wherein different voltages [fig. 5, power and ground connected to "R1" and "R2", and "52" and "54"] supplied to the two voltage source lines are applied to said pixel electrode based on the information stored by the corresponding memory circuit, and

wherein said memory circuit comprises at least second [fig. 5, "54"] and third thin film transistors [fig. 5, "52"], one of source or drain of the second thin film transistor [fig. 5, "54"] being connected with one of two voltage source lines [fig. 5, the line delivering the power to the resistor"] through a first resistor [fig. 5, "R4"], a gate electrode of the third thin film transistor [fig. 5, "52"], and one of source or drain of the first thin film transistor [fig. 5, "38"],

the other of source or drain of the second transistor [fig. 5, "54"] being connected with the other of two voltage source lines [fig. 5, the line delivering the ground to "54"] and one of source or drain of the third thin film transistor [fig. 5, "52", note that all grounds are connected] and

a gate electrode of the second thin film transistor [fig. 5, "54"] being connected with the other of source or drain of the third thin film transistor [fig. 5, "52"], one of two voltage source lines through a second resistor [fig. 5, "R2"], and said pixel electrode [fig. 5, "36"].

Parks does not teach that an AC voltage having an amplitude equivalent to that of the voltages output of the memory circuit is supplied to the opposite electrode.

However, Hoshi teaches the concept of providing an AC voltage [fig. 3a, "12b"] having an amplitude equivalent to that of the voltage output [fig. 3a, "12a"] of a memory circuit [fig. 2, "7" and "8"] in an active matrix display device [fig. 2] to an opposite electrode [fig. 2, the electrode corresponding to the bottom portion of "9"] of the display device [col. 5, the last eight lines].

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to output a first AC voltage from the memory circuit of Parks and to output a second AC voltage having an amplitude equivalent to that of the voltage output of the first AC voltage from the opposite electrode, as taught by Hoshi, in order to achieve the predictable result of reducing power consumption and preventing the degradation of the electro-optical modulating layer.

As to **claim 25**, Parks as modified by Hoshi teaches that a voltage supplied to the electro-optical modulating layer is substantially zero on time average [Hoshi, figs. 3a-3b].

As to **claim 26**, Parks as modified by Hoshi teaches that the number of pixel electrodes [Parks, fig. 5, "36"] equals the number of the memory circuits [Parks, fig. 5, "50" excluding "38"].

As to **claim 29**, Parks teaches that the different voltages [Parks, fig. 5, power and ground connected to "R1" and "R2", and "52" and "54"] include a high voltage and a low voltage.

As to **claim 48**, Parks teaches that said electro-optical modulating layer comprises a liquid crystal [abs., l. 1].

As to **claim 50**, Parks teaches that said electro-optical modulating layer comprises a liquid crystal [abs., l. 1].

Claim 27 is rejected under 35 U.S.C. 103(a) as being unpatentable over Parks and Hoshi as applied to claims 12-14, 17, 24-26, 29, 48, and 50 above, and further in view of Johary.

Parks as modified by Hoshi does not expressly teach that the active matrix display device includes a digital gradation display device.

However, Johary teaches the concept of generating a digital gradation signal [fig. 1d] as the display signal for a display device.

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify the active matrix display device of Parks as modified above to use a digital and time gradation signal as the display signal, as taught by Johary, in order to provide an effective visual differentiation for displayed images [Johary, col. 1, ll. 28-32].

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event,

however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to SEOKYUN MOON whose telephone number is (571)272-5552. The examiner can normally be reached on 8:30 am - 5:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sumati Lefkowitz can be reached on (571)272-3638. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

August 5, 2012
/Seokyun Moon/
Primary Examiner, Art Unit 2629